A 75 W TV Power Supply Operating in Quasi-square Wave Resonant Mode using the NCP1207 Controller

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APPLICATION NOTE

Introduction

Quasi−square wave resonant converters, also known as quasi−resonant (QR) converters, allow designing flyback Switch−Mode Power Supplies (SMPS) with reduced Electro−Magnetic Interference (EMI) signature and improved efficiency. Due to the low level of generated noise, QR SMPS are therefore very well suited to applications dealing with RF signals, such as TVs.

ON Semiconductor NCP1207 is a QR controller that will ease your design of an EMI−friendly TV power supply with only a few additional components, and able to lower its standby power down to 1.0 W.

What is Quasi−Resonance?

The term quasi−resonance is normally related to the association of a real hard−switching converter and a resonant tank. While the operation in terms of control is similar to that of a standard PWM controller, an additional network is added to shape the variables around the MOSFET: current or voltage. Depending on the operating mode, it becomes possible to either switch at zero current (ZCS) or zero voltage (ZVS). Compared to a conventional PWM converter, a QR operation offers less switching losses but the RMS current circulating through the MOSFET increases and forces higher conduction losses; with a careful design, efficiency can be improved. However, one of the main advantages in favor of the quasi−resonance is the reduced spectrum content either conducted or radiated.

True ZVS quasi−resonance means that the voltage present on the switch looks like a sinusoidal arch. Figure 1 shows how such a signal could look like.

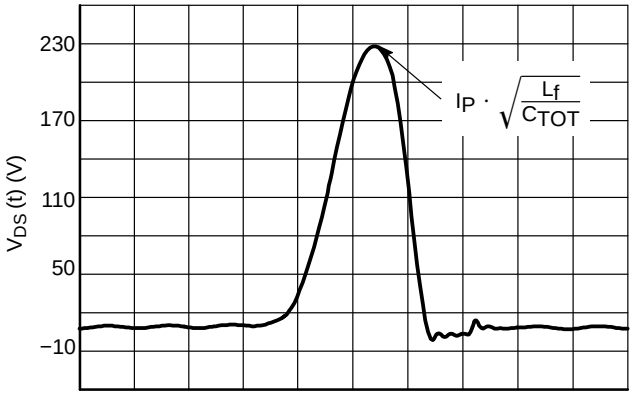

Figure 1. A Truly Resonating V_{DS} Signal on a Quasi−resonant Flyback Converter

The main problem with this technique lies in the very high voltage generated at the switch opening. Most of the time, these resonant offline designs require around 1.0 kV BVdss MOSFETs whose price is clearly incompatible with high volume markets. As a result, designers orientate their choice toward another compromise called quasi−square wave resonant power supply.

Quasi−Square Wave Resonant Converters

As we saw, true resonant operation put a constraint on MOSFET selection by imposing a high voltage at the switch opening. If we closely look at the standard hard−switching waveform (Figure 2), we can see that at a given time the drain voltage goes to a minimum. This occurs just after the core reset.

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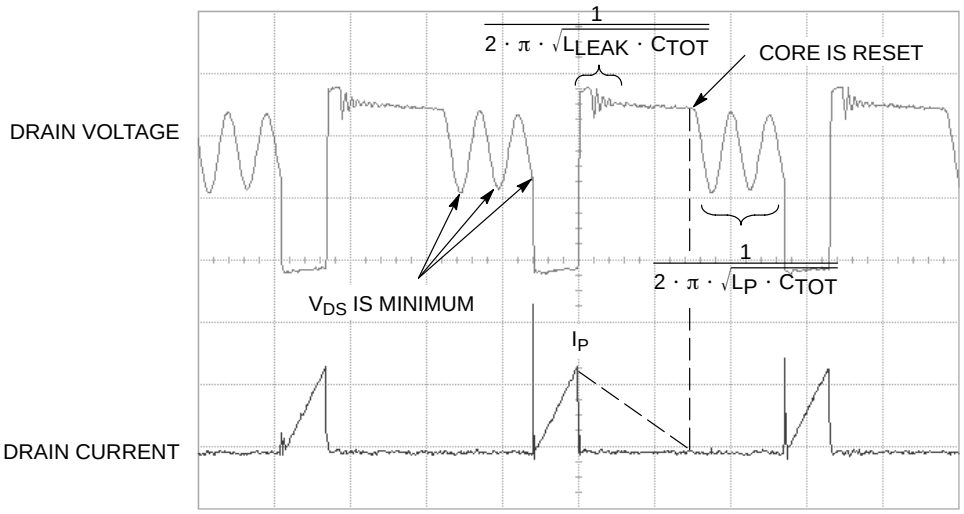


Figure 2. Hard−switching Waveforms in Discontinuous Conduction Mode (DCM)

From Figure 2, it is possible to imagine a controller that turns a MOSFET ON until its current grows−up to the setpoint. Then it turns the MOSFET OFF until the core reset is detected (usually via an auxiliary winding). As a result, the controller does not include any stand alone clock but only detects the presence of events conditioned by load/line conditions: this is a so−called free−running operation. Converters based on this technique are often designated as Self−Oscillating Power Supplies (SOPS), valley switching converters, etc.

Oscillations origins can be seen from Figure 3 arrangement where L−C networks appear.

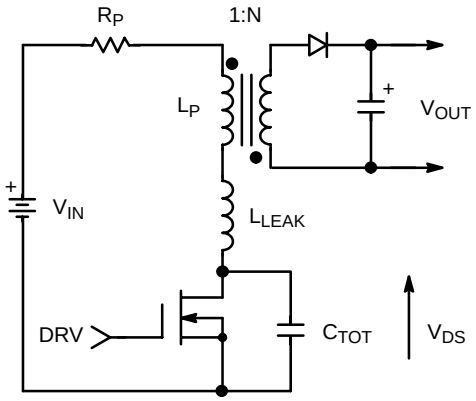


Figure 3. A Typical Flyback Arrangement Shows Two Different Resonating Networks

Depending on the event, two different configurations are seen:

- At the switch closing, the primary current flows through the primary inductance L_P but also the leakage inductance, L_{LEAK}. When the turn−on time expires, the energy stored in L_P is transferred to the secondary side of the transformer via the coupling flux. However, the leakage inductance, which models the coupling between both transformer sides, reverses its voltage and imposes a quickly rising drain voltage. The slope of this current is $\frac{I_P}{C_{TOT}}$ (eq. 1) where C_{TOT} gathers all capacitors surrounding the drain node: MOSFET capacitors, primary transformer parasitic capacitors but also those reflected from the secondary side, etc. As a result, L_{LEAK} together with C_{TOT} form a resonating network of natural frequency $\frac{1}{2 \cdot \pi \cdot \sqrt{L_{LEAK} \cdot C_{TOT}}}$ (eq. 2). The maximum drain voltage can then be computed using the characteristic impedance of this LC network:

$$V_{DS\ max} = V_{IN} + \frac{1}{N} \cdot (V_{OUT} + V_F) + I_P \cdot \sqrt{\frac{L_{LEAK}}{C_{TOT}}} \quad \text{(eq. 3)}$$

- When the transformer core resets, primary and secondary currents drop to zero. The secondary diode stops its conduction and the reflected voltage on the primary naturally dies out. From equation 3, this means that terms after V_{IN} all collapse to zero and V_{DS} tends toward V_{IN}. However, the transition would be brutal in the lack of a resonating network, this time made by L_P, the primary inductance, and nearly the same C_{TOT} as before. A sinusoidal ringing takes place, damped by the presence of ohmic losses (DC + AC resistance of the primary winding, modeled by R_P). The drain−source shape rings as the formula below details:

$$V_{DS}(t) = V_{IN} + \frac{1}{N} \cdot (V_{OUT} + V_F) \cdot e^{-a \cdot t} \cdot \cos(2 \cdot \pi \cdot F_{PRIM} \cdot t) \quad \text{(eq. 4)}$$

with: $a = \frac{R_P}{2 \cdot L_P}$ (eq. 5) the damping factor

$$F_{PRIM} = F_{PRIM} = \frac{1}{2 \cdot \pi \cdot \sqrt{L_P \cdot C_{TOT}}} \quad \text{(eq. 6)}$$

the natural ringing frequency

V_{IN} the input voltage, V_F the diode's forward drop and N the $= \frac{N_S}{N_P}$ turn ratio.

We can see from Figure 4 that the drain is the seat of various local minimums when going along the ringing wave. These drops are called "valleys". If we manage to switch the MOSFET right in the middle of these valleys, we ensure minimum turn−on losses, particularly those related to capacitive dissipation:

$$P_{avg_{CAP}} = \frac{1}{2} \cdot C_{TOT} \cdot V_{DS}^2 \cdot F_{SW} \quad \text{(eq. 7)} \rightarrow 0.$$

Thus, quasi−square wave operation (or valley switching) will imply a re−activation of the switch when VDS is minimum. As various figures portray, this occurs some time further to the transformer core reset. By implementing this method, we build a converter that naturally exhibits a variable frequency operation since the reset time depends upon the input/output operating conditions. Figure 5 shows a typical shot of a quasi−square wave converter.

As one can see, the total period is made of different events, where the core is first magnetized (T_{ON}), then fully reset (T_{OFF}) and finally a time delay (T_W) is inserted to reach the lowest value on the drain. Let us look at how the frequency moves by respect to the input/output conditions.

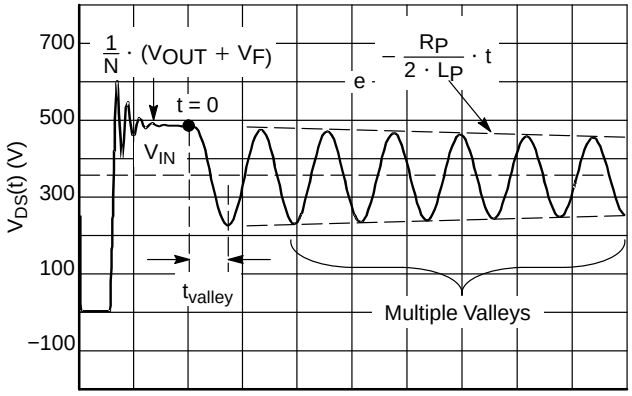


Figure 4. A Typical Flyback Ringing Waveform Occurring at the Switch Opening

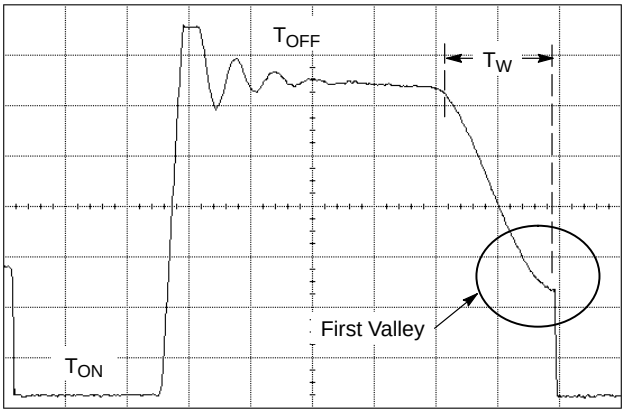


Figure 5. A Typical Drain−Source Shot of a Quasi−square Wave Converter

Evaluating the Free−Running Switching Frequency

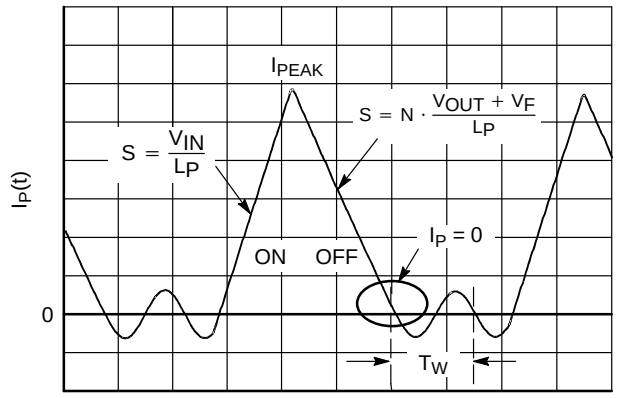


Figure 6. The Primary Inductance Current is made of Two Different Slopes

The free−running frequency can be evaluated by looking at Figure 6, where the primary current (circulating in the primary inductance) is depicted. From the definition of the various slopes, we can express the first two events, T_{ON} and T_{OFF} quite easily:

$$T_{ON} = \frac{L_P}{V_{IN}} \cdot I_P \quad \text{(eq. 8)}$$

$$T_{OFF} = \frac{L_P}{\left[\frac{N_P}{N_S} \cdot (V_{OUT} + V_F)\right]} \cdot I_P \quad \text{(eq. 9)}$$

For the T_W event, which is one fourth of the natural ringing frequency given by equation 4, we will compute the derivative of equation 4 and null it to find its minimum:

$$\frac{d\,(V_{IN} + e^{-a \cdot t} \cdot \cos\,(2 \cdot \pi \cdot F_{PRIM} \cdot t))}{dt} = 0 \quad \text{(eq. 10)}$$

Which gives a result of:

$$T_W = \frac{1}{2 \cdot ft} - \frac{1}{2} \cdot \frac{a \cdot \tan\left[\frac{a}{2 \cdot \pi \cdot F_{PRIM}}\right]}{\pi \cdot F_{PRIM}} \quad \text{(eq. 11)}$$

However, this result is not very practical because of its inherent complexity. If we observe equation 10, we can see that the minimum is reached when the term $\cos\,(2 \cdot \pi \cdot F_{PRIM} \cdot t)$ equals −1. Otherwise stated, we can solve t for which the cosine is equal to zero, or the full product equals π. This gives:

$$T_W = \frac{1}{2 \cdot F_{PRIM}} = \pi \cdot \sqrt{L_P \cdot C_P} \quad \text{(eq. 12)}$$

However, this result is valid only for low damping coefficient, that is to say, $e^{-a \cdot t} \approx 1$. Experience shows that it is good enough for the vast majority of cases.

As a result, the final switching period is computed by summing up all these sequences and introducing the input power expression: $T = T_{ON} + T_{OFF} + T_W$. (eq. 13)

$$T_{ON} + T_{OFF} + T_W = I_P \cdot L_P \cdot \left[\frac{1}{V_{IN}} + \frac{1}{\left[\frac{N_P}{N_S} \cdot (V_{OUT} + V_F)\right]}\right] + \pi \cdot \sqrt{L_P \cdot C_P} = \frac{1}{F_{SW}} \quad \text{(eq. 14)}$$

$$P_{IN} = \frac{P_{OUT}}{\eta} = \frac{1}{2} \cdot L_P \cdot I_P{}^2 \cdot F_{SW} \quad \text{(eq. 15)}$$

from equation 15, $I_P = \sqrt{\frac{2 \cdot P_{OUT}}{\eta \cdot L_P \cdot F_{SW}}}$ (eq. 16).

Now, plugging F_{SW} in equation 16 gives:

$$I_P \cdot L_P \cdot \left(\frac{1}{V_{IN}} + \frac{1}{V_{REFLECT}}\right) + T_W = \frac{L_P \cdot I_P{}^2 \cdot \eta}{2 \cdot P_{OUT}} \quad \text{(eq. 17)}$$

with: $V_{REFLECT} = \frac{N_P}{N_S} \cdot [V_{OUT} + V_F]$

$T_W = \pi \cdot \sqrt{L_P \cdot C_P}$

η the converter efficiency

P_{OUT} the output power

V_{OUT} and V_F, respectively the output voltage and the rectifier drop @ $I_D = I_{OUT}$

L_P the primary inductance.

Stating that: $2 \cdot L_P \cdot P_{OUT} = A$;

$$I_P = \frac{\left(A \cdot V_{REFLECT} + A \cdot V_{IN} + \sqrt{A \cdot (V_{REFLECT}{}^2 + 2 \cdot A \cdot V_{REFLECT} \cdot V_{IN} + A \cdot V_{IN}{}^2 + 2 \cdot \eta \cdot V_{IN}{}^2 \cdot V_{REFLECT}{}^2 \cdot T_W)}\right)}{\eta \cdot L_P \cdot V_{IN} \cdot V_{REFLECT}} \quad \text{(eq. 18)}$$

From equation 16, we can then compute the switching frequency using the calculated peak current:

$$F_{SW} = \frac{2 \cdot P_{OUT}}{\eta \cdot L_P \cdot I_P^2} \quad \text{(eq. 19)}$$

However, equation 18 is not very practical since it involves L_P, what we are actually looking for... It can certainly be used to discover the operating peak current from known inductance and capacitor values. But neglecting T_W, a simpler formula can be used as first frequency iteration (e.g. to feed a SPICE simulator for instance):

$$I_P = 2 \cdot P_{OUT} \cdot \frac{V_{REFLECT} + V_{IN}}{\eta \cdot V_{IN} \cdot V_{REFLECT}} \quad \text{(eq. 20)}$$

$$F_{SW} = \frac{1}{L_P \cdot 2 \cdot P_{OUT} \left(\frac{N \cdot (V_{OUT} + V_F) + V_{IN}}{\eta \cdot (V_{IN} \cdot (N \cdot (V_{OUT} + V_F)))} \right)^2} \quad \text{(eq. 21)}$$

Entering equation 21 into a spreadsheet and plotting F_{SW} versus various parameters (V_{OUT}, I_{OUT}, etc.) gives an idea about the high frequency variability of the system. Figure 7 and Figure 8 respectively plot F_{SW} in function of the input voltage and the output current for a given application.

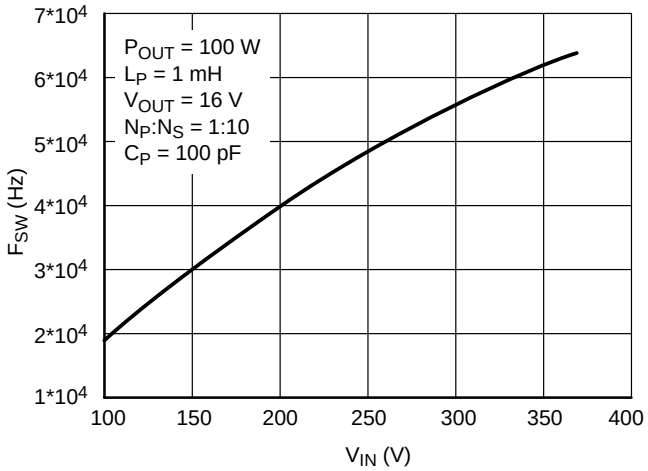


Figure 7. Frequency Variations for a 100 W SMPS Operated from a Universal Mains

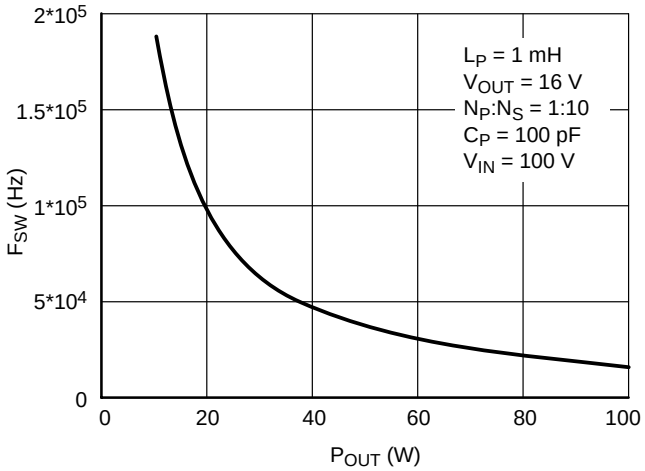


Figure 8. Frequency Dependency with Load at a Given Input Voltage (100 V)

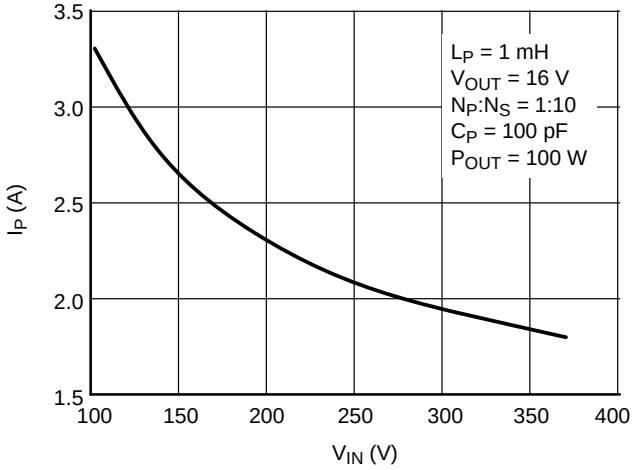


Figure 9. Peak Current Variations for a 100 W Output Power with Different Line Voltages

A Quiet EMI Signature

Manipulating sinusoidal (or close−to) variables always offer a narrower spectrum content compared to hard−switching systems. Figure 10 and Figure 11 depict the conducted EMI signature of two systems operated at the same point but implementing different switching techniques.

Since the MOSFET is re−activated at the lowest drain level, the classical C_{OSS} capacitor discharge at the switch closing does not exist and the very narrow peak current has gone (also this peak is often confusing the current−sense comparator when it is really energetic, even sometimes despite the presence of the LEB circuitry). As a result, Quasi−square wave converters are recommended where the Switch−Mode Power Supply (SMPS) needs to operate close to Radio−Frequency section, notably in TV chassis.

Detecting the Core Reset Event

Core reset detection is usually done via a dedicated auxiliary winding whose voltage image is directly linked to the transformer flux by:

$$V_{AUX} = N \cdot \frac{d\varphi}{dt} \qquad \text{(eq. 22)}$$

Depending on the controller device, the polarity of the observed signal must fit its detection circuitry. In ON Semiconductor NCP1207, this polarity should be of Flyback type, that is to say, when the MOSFET closes, the auxiliary voltage dips below ground and stays there, safely clamped at −0.7 V, until the MOSFET is turned off. Figure 12 gives an example of the demagnetization signal for NCP1207.

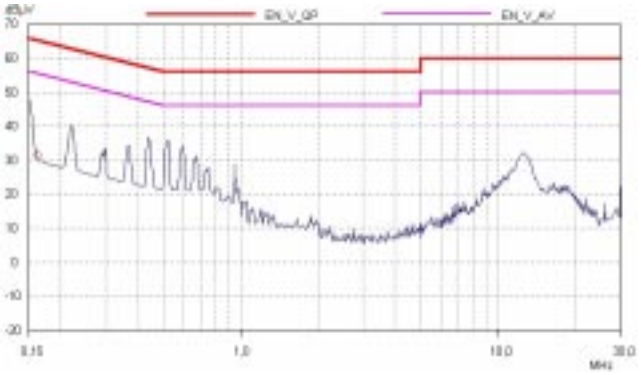


Figure 10. A Soft−switching Approach Reduces the Energy Content Above 1 MHz

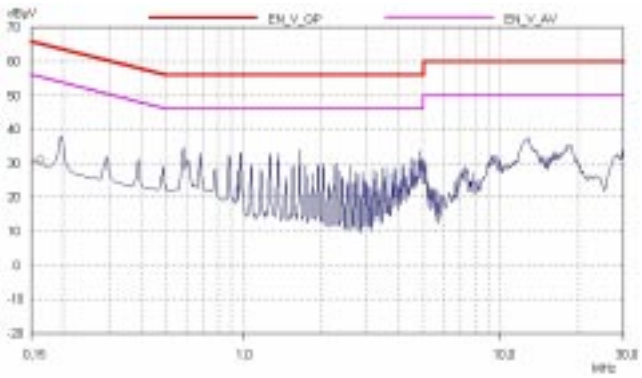


Figure 11. A Hard−switching System Generates a lot of Noise in the Same Portion

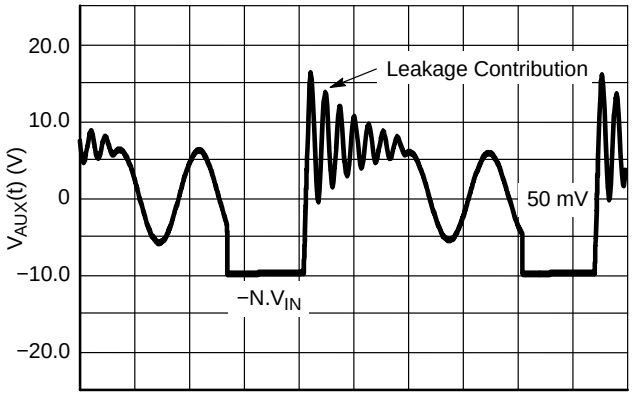


Figure 12. Core Reset Detection Signal Coming from a Flyback Winding

The NCP1207 Quasi−resonant Controller

Quasi−square Wave Resonant Operation: Due to its dedicated pin, NCP1207 is able to detect the end of the transformer core demagnetization before starting a new switching cycle. The closing of the MOSFET thus occurs at zero current, cutting out switch turn−on losses and secondary diode recovery losses. By delaying the turn−on event, it is possible to turn the MOSFET on in the minimum of the drain−source wave, further reducing the losses and the electromagnetic interference (EMI). NCP1207 also features a minimum T_{OFF}, preventing a frequency runaway at light loads: when the demagnetization occurs before the end of the blanking delay, the device waits for the next valley before enabling a new cycle.

Low Standby Power: When the output power demand decreases, the feedback (FB) pin voltage decreases at the same time. When it becomes lower than the selected threshold, the device starts to skip cycles, generating just enough switching pulses to maintain the output voltage. This cycle skipping only occurs at low peak current, ensuring a noise−free standby operation.

Short−circuit Protection: The IC permanently monitors the feedback line activity, ready to enter a safe burst mode if it detects a short circuit. Once the short−circuit has disappeared, the controller automatically goes back to normal operation.

OVP Protection: By sampling the plateau voltage of the demagnetization winding, the NCP1207 is able to detect an over voltage on the output. In this case the IC goes in fault, permanently disabling the output. This protection is fully latched, which means that the power supply has to be unplugged from the mains to unlatch it.

External MOSFET Connection: By leaving the MOSFET external from the IC, you can choose the device exactly suited for your application. You also have the ability to control the shape of the gate signal, giving you an additional way to reduce the amount of EMI and video noise.

SPICE Model: A free−running model allows running transient cycle−by−cycle simulations to verify theoretical design and help to speed up the design stage of a power supply. An averaged model dedicated to AC analysis is also available to ease the stabilization of the loop. Ready−to−use templates can be downloaded in OrCAD's PSpice and Intusoft's ISPICE from ON Semiconductor web site, NCP1207 related section.

The data sheet gives complete details regarding the implementation of the NCP1207.

A 75 W TV Power Supply Design

Power Supply Specification

Input Voltage	Universal input 90 VAC to 265 VAC
Output Power	60 to 75 W
Outputs	+108 V 500 mA max (54 W) Regulated +12 V 920 mA max (11 W) −12 V 670 mA max (8.0 W) +5 V 70 mA derived from +12 V through a regulator +3.3 V 50 mA derived from +5.0 V through a regulator
Protections	Short−circuit, over−voltage and over−power
Standby Power	Below 1.0 W

Design Steps

1. **Reflected Voltage**

   Let us first start the design by selecting the amount of secondary voltage we want to reflect on the primary side, which will give us the primary to secondary turn ratio of the transformer. If we decide that we want to use a rather cheap and common 600 V MOSFET, we will select the turn ratio by:

   $$V_{IN\,max} + N \cdot (V_{OUT} + V_F) < 600\ V$$

   V_{INmax} is 370 V and $(V_{OUT} + V_F)$ is about 110 V. If we decide to keep a 10% safety margin, it gives $N < 1.5$. We will choose a turn ratio of $N = 1.2$, which will give a reflected voltage of 130 V.

2. **Peak Current**

   Knowing the turn ratio, we can now calculate the peak primary current needed to supply the 75 W of output power. If we neglect the delay T_W between the zero of the current and the valley of the drain voltage, we can calculate I_{Pmax} (from equation 20) by:

   $$I_{Pmax} = 2 \cdot P_{OUT} \cdot \frac{V_{INmin} + N \cdot (V_{OUT} + V_F)}{\eta \cdot N \cdot V_{INmin} \cdot (V_{OUT} + V_F)}$$

   V_{INmin} is 110 V and η is 85%. Plugging the other values gives us a maximum peak current of $I_{Pmax} = 2.96$ A. We will choose a value of 3.5 A to take into account various tolerances. NCP1207 max current sense setpoint is 1.0 V, so we should put a sense resistor $R_S = \frac{1.0\ V}{3.5\ A} = 0.286\ \Omega$. We will use four standard 1.1 Ω resistors in parallel.

3. **Primary Inductance**

To calculate the primary inductance L_P, we need to decide the switching frequency range we allow the controller to operate. There are two constraints; at low line, maximum power, the switching frequency should be above the audible range (higher than 20 kHz), at high line, lowest nominal power, the OFF time (T_{OFF} + T_W) of the MOSFET should be higher than 8.0 μs, to prevent the controller to jump between valleys (because these discrete jumps between 2 valleys can generate noise in the transformer as well). If we still neglect T_W, L_P is then given by (equation 19):

$$L_P \leq \frac{1}{2 \cdot F_{SWmin} \cdot P_{OUTmax} \cdot \left(\frac{V_{INmin} + N \cdot (V_{OUT} + V_F)}{\eta \cdot N \cdot V_{INmin} \cdot (V_{OUT} + V_F)}\right)^2}$$

If we choose 25 kHz min for 75 W of output power at 110 Vdc, we obtain: $L_P \leq 687$ μH.

To take tolerances into account, we can choose L_P = 600 μH, and verify if it satisfies the second condition:

For 60 W output power at 375 Vdc, I_P = 1.46 A. From equation 9, T_{OFF} = 6.74 μs.

If we connect a 330 pF drain−to−source capacitor, we calculate T_W from equation 12: T_W = 1.4 μs.

T_{OFF} + T_W = 8.14 μs, which is higher than 8.0 μs.

If nominal output power range of the power supply is wider, we can choose a higher L_P (650 μH for instance) or increase C_{DRAIN}. But this last solution will decrease efficiency, as V_{DS} is not equal to 0 when the MOSFET is turned on: in this case Zero Voltage Switching (ZVS) can be a good choice (see below).

4. **Clamp**

In equation 3, we can calculate the overvoltage due to the leakage inductance: $V_{OV_{LEAK}} = I_P \frac{\sqrt{L_{LEAK}}}{C_{TOT}}$.

At this time we don't know the value of L_{LEAK}, but we can choose a value of 2% of the primary inductance (i.e. 12 μH), which would not be too far from the final value. Considering again 330 pF on the drain, at 375 V input voltage and 75 W of output power, which give I_P = 1.83 A, we obtain $V_{OV_{LEAK}}$ = 349 V.

But we only have 95 V available before reaching the MOSFET breakdown voltage. So we will need to add a clamp to limit the spike at turn−off.

Please refer to application note AN1679/D (available at www.onsemi.com) to calculate this clamp. You can also use a SPICE simulator to test the right values for the components.

We chose to use an RCD clamp, using a 1N4937 diode with a 220 pF snubber capacitor, a 47 kΩ resistor and a 10 nF capacitor: it is an aggressive design (the maximum drain voltage will be very close to the maximum voltage allowable for the MOSFET), but it gives enough protection without degrading too much the efficiency.

Once again, if we design the SMPS to work in ZVS, we can have a bigger drain capacitor, that will damp the leakage inductor effect (see below).

Same Calculation (1 to 4) for a ZVS Power Supply:

Let us start the design from the beginning, to implement a true ZVS: if we decide to reflect 300 V, assuming that we have an 800 V MOSFET, we will have a turn ratio of 2.8. The exact reflected voltage will be 308 V, and the available margin for leakage inductance effect will be 117 V. I_{Pmax} will then be equal to 2.18 A. Applying the same conditions for L_P will give $L_P \leq$ 1.26 mH. If we choose 1.0 mH, C_{DRAIN} should be higher than 1.6 nF to avoid valley jumping at 375 Vdc for a 60 W output consumption. If we want to avoid the use of a clamping network to protect the MOSFET, C_{TOT} should be higher than 2.05 nF (stating that L_{LEAK} = 25 μH, and that the maximum overvoltage due to leakage inductance is 115 V). We can choose a capacitor C_{DRAIN} = 2.2 nF to be safe.

You can see through the lines we wrote that many parameters could be changed to obtain different converters at the end. The reflected voltage is obviously one of the most sensitive parameters that influence others. Increasing the reflected voltage to keep a wider ZVS operating range has a price on other numbers:

- The switching frequency increases (reset voltage on L_P is stronger)
- The primary peak current and conduction losses are improved (if F_{SW} goes up, the peak demand goes low)
- The secondary peak current and conduction losses increase
- The MOSFET undergoes a bigger stress at the switch opening
- MOSFET turn−on losses can be really null (if ZVS is achieved).

To simplify the design of your power supply, a spreadsheet (that includes all the parasitic elements) is available to download from the ON Semiconductor web site (www.onsemi.com), under NCP1207 page. The formulae are described in the application note AND8089/D. You can also simulate the complete power supply in a SPICE simulator, using the NCP1207 models also available from the website.

5. **SPICE Simulation**

The faster and easier way to simulate this power supply is to use a simplified free−run model to have an idea of the final results. Figure 13 offers a possible way to represent a free−running controller: the demagnetization path includes a standard flip−flop that latches the transition while the feedback signal fixes the current setpoint. Due to a simple arrangement, the system simulates very quickly and allows an immediate assessment of what has been suggested by the Excel spreadsheet. The feedback loop is purposely simplified with a Zener diode arrangement, but you can upgrade it with a TL431 circuitry. It will simply take longer simulation time to settle.

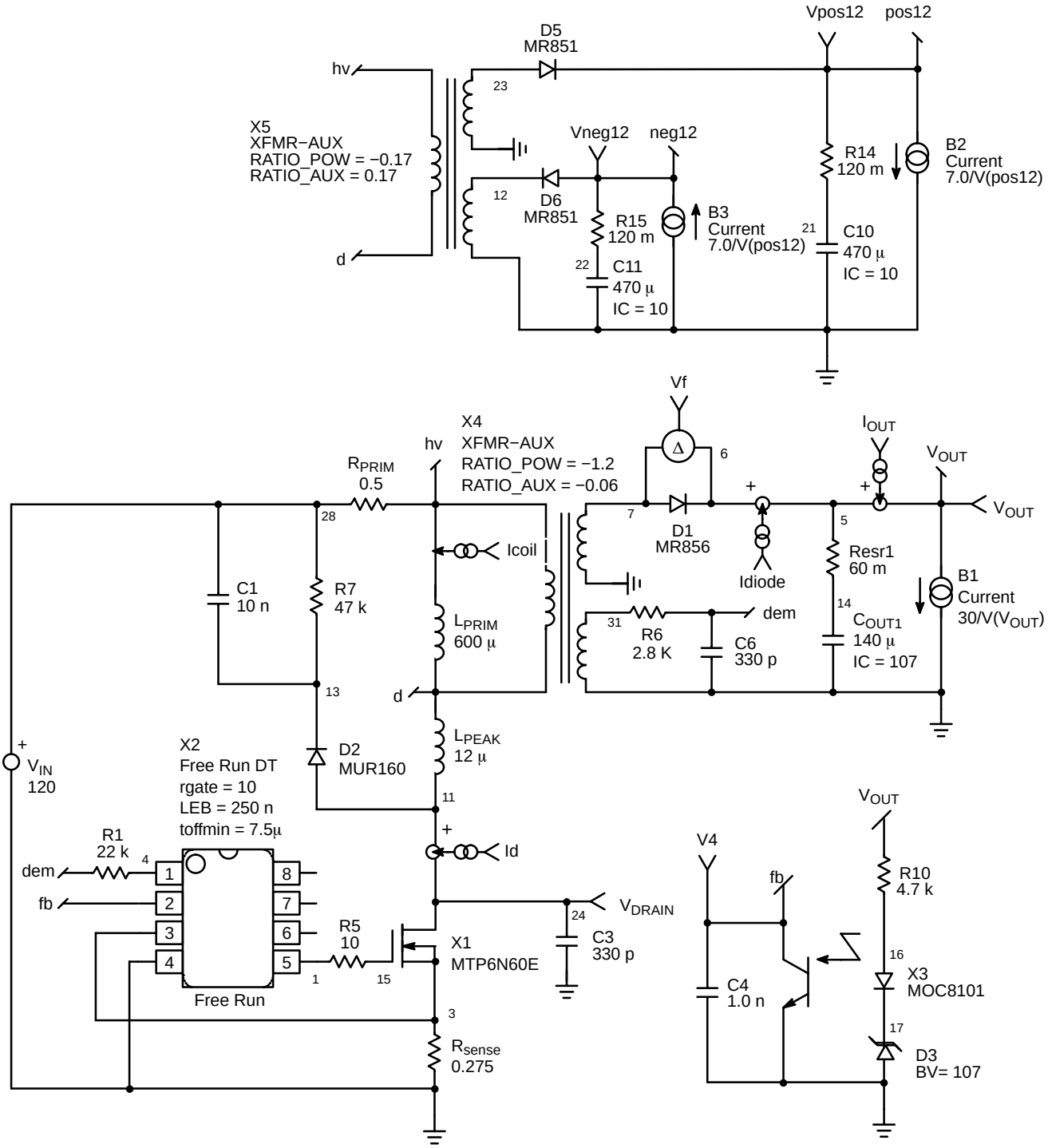


Figure 13. Simulation Schematic of the TV Power Supply

As Figure 14 and Figure 15 show, the simulation is very close to what is obtained on the board:

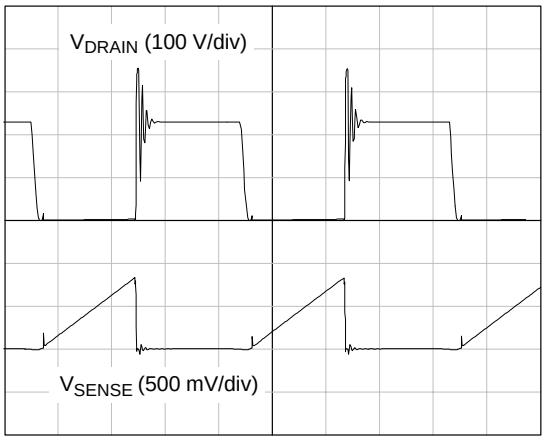


Figure 14. Simulation Results

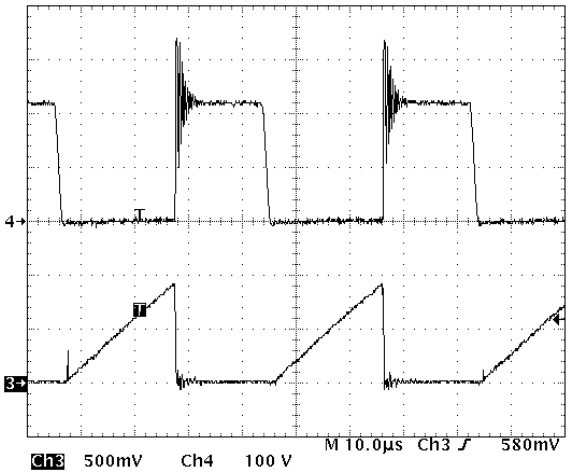


Figure 15. Real Measurements

The SPICE simulation offers another advantage, which is the evaluation of the component stresses. Due to good models, you can immediately measure the MOSFET conduction losses worse case, the RMS current in the rectifiers, in the resonating capacitor and in the output capacitors, and choose the right components accordingly.

For instance we used the simulated RMS currents to determinate the winding characteristics of the transformer, knowing that low line imposes the highest stress on the transformer. Based on the simulation results, the following specification has been sent to the transformer manufacturer:

Primary: Input voltage: 90 VAC to 275 VAC
Switching frequency: 30 kHz to 80 kHz
L_P = 600 µH
I_{Ppeak} = 3.6 A
$I_{P\ RMS}$ = 1.3 A

Aux: ratio N_P/N_{AUX} = 9.0, I_{RMS} = 10 mA

Secondaries:
B+ (+108 V): ratio N_P / N_{B+} = 1.0, I_{RMS} = 1.0 A
POW1 (+12 V): ratio N_P / N_{POW1} = 9.0, I_{RMS} = 1.2 A
POW2 (−12 V): ratio N_P / N_{POW2} = 9.0, I_{RMS} = 900 mA

6. **Auxiliary Winding**

The auxiliary winding will be used to supply the controller and to detect the transformer demagnetization. To supply V_{CC}, the voltage should be higher than 11 V (V_{CCOFF} + V_F), but lower than 16 V (max voltage to be applied on V_{CC} pin): we can choose a value of 12 V.

The voltage applied on demagnetization pin (pin 1) should be lower than the over−voltage protection (OVP) threshold, which is 7.2 V. We will add an external resistor to divide the auxiliary voltage by 2: the plateau voltage during normal operation will be 6.0 V. It will allow a 2.4 V over−voltage on the auxiliary winding, corresponding to a 21.6 V over−voltage on +108 V output, which is acceptable.

There is an internal 28 k resistor, so we just need to add another external 28 k, or 27 k for a more standard value. There is an internal clamping diode to protect pin 1 against lethal over−voltages, and the current in this diode should never be higher than +3 mA/−2 mA: we must verify that the chosen resistor is in accordance with this specification. If during turn−on, the auxiliary winding delivers 35 V (at the highest line level), then the maximum current flowing from pin 1 is: (35 V + 0.7 V)/27 kΩ = 1.32 mA, which is safe.

This resistor, which connects the winding to the pin (called R_{OVP1} on the schematic), will also be used to delay the turn−on of the MOSFET to be sure to be right in the valley of the drain voltage. If the total internal capacitance of pin1 (10 pF) is not giving enough delay, an external capacitor will be added. In our case, we will add a 82 pF capacitor, which will delay the turn−on exactly in the valley.

7. **DSS**

The main reason why the auxiliary winding will also be used to supply the controller is that the maximum total gate charge of a 6.0 A, 600 V MOSFET can be as high as 50 nC. Knowing that the current consumed by the output stage is $I_{DRV} = F_{SW} \times Q_g \times V_{DRV}$, even for a 20 kHz frequency and V_{DRV} = 10 V, I_{DRV} will be higher than 10 mA. And this current will directly flow through the DSS if no auxiliary supply is used.

Nevertheless, the DSS is of great interest in a TV power supply. When a secondary reconfiguration is used (or at least the regulation point is lowered) to reduce the standby power, the auxiliary voltage collapses. Due to the DSS, the controller is still fully powered during standby. This allows to regulate at the lowest possible voltage (minimum input voltage of the standby regulator), and the transition from standby to normal mode is smoother (see measurements section of this document).

The high voltage pin will be connected to one of the mains inputs through a simple 1N4007 diode to lower the standby power, due to the reduced average voltage due to half−wave rectification (see NCP1207 data sheet for details).

8. **Standby**

The standby consumption should be below 1.0 W. To achieve this target, the secondary current consumption should be reduced. We choose to use a secondary reconfiguration that, by re−routing the high voltage winding to the low voltage output, reduces the voltage of all the unused outputs. The reconfiguration is made by a thyristor, activated by a manual switch to simplify the use of the evaluation board (see Figure 16).

In fact, the energy stored in the high voltage winding is used to refuel the low voltage output capacitor, and regulation is now made on this low voltage output. As the windings are imposing currents (not voltages), connecting a high voltage winding to a low voltage output is completely safe. But as the regulation loop now forces the high voltage winding to deliver a low voltage, then all the other windings are also delivering lower voltages than in normal conditions (in the same ratio). The sum of the consumptions on all the windings is drastically reduced due to this division of all the output voltages.

During standby, the regulation is made through the Zener diode DZ2 (Figure 17). As NCP1207 is still powered due to the DSS, even is there is no more auxiliary voltage, the regulation point can be lower than in normal mode. The only constraint for the output voltage is to be higher than the minimum input voltage of the voltage regulator, but there is no need for any guard band. To regulate the 5.0 V output, we use a standard MC7805 in TO220, with a drop voltage of 2.0 V: the regulation point can be as low as 7.0 V. R9 and C22 can be added to soften the transitions between standby and normal modes. They are usually not necessary if the loop compensation is correctly designed (by adding RC networks around the TL431).

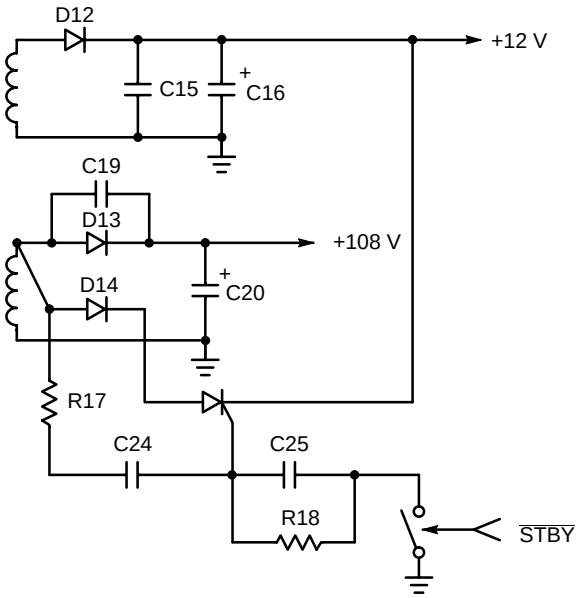


Figure 16. Secondary Reconfiguration with Thyristor

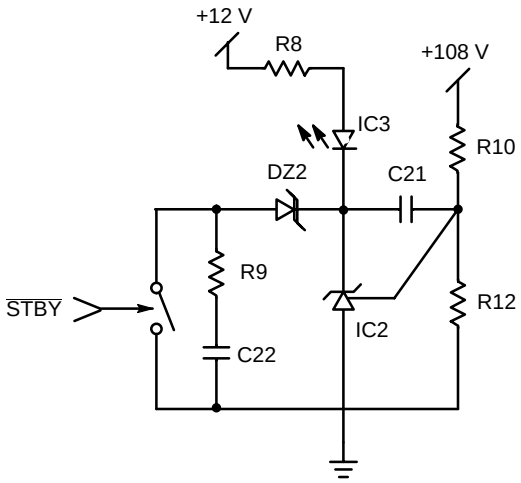


Figure 17. Standby Regulation for Secondary Reconfiguration

The NCP1207 enters a low peak current skip mode to lower the consumption in low−load conditions. But with some cheap transformers, the peak current might be too high, generating an audible noise. In that case, we propose a different implementation for the standby regulation (Figure 18): by imposing a ripple on the regulated output, we force the controller to run in a burst mode, which generates less mechanical stress in the transformer.

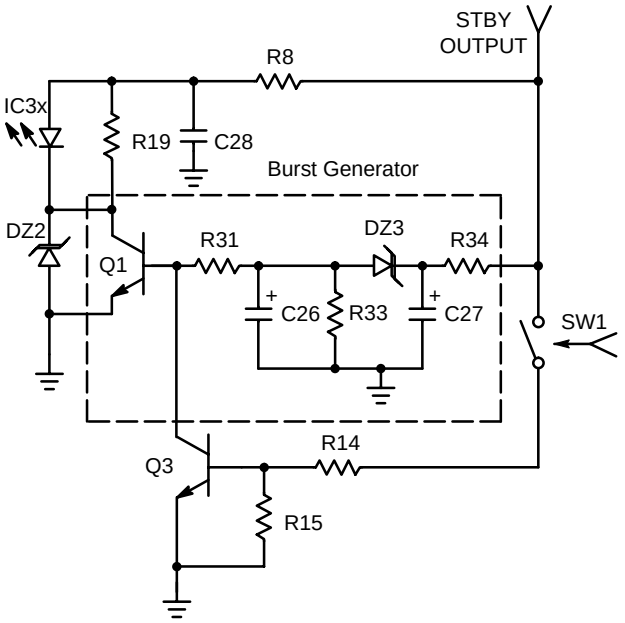


Figure 18. This Standby Regulation Circuitry Imposes a Noise−free Burst Mode

9. **Overpower Protection**

NCP1207 integrates a short−circuit protection, based on the sensing of the peak primary current. Unfortunately, as we have seen before, this peak current is dependent of the input voltage (Figure 19): the sense resistor has to be chosen to allow the maximum peak current at low input voltage to flow in the MOSFET. But at high input voltage, the peak current necessary to deliver the same output power is much lower: the sense resistor being fixed, the maximum output power deliverable at high input voltage is much greater. The conclusion is that the built−in short−circuit protection is not an overpower protection (OPP).

It is however possible to implement an OPP by adding few additional components beside the controller. We propose two different approaches, one by compensating the CS pin voltage depending on the input voltage, the other by sensing the output current.

Approach 1 (Overpower Compensation):

A classical way to compensate this effect is to add an amount of the input voltage to the primary current sense information (Figure 19):

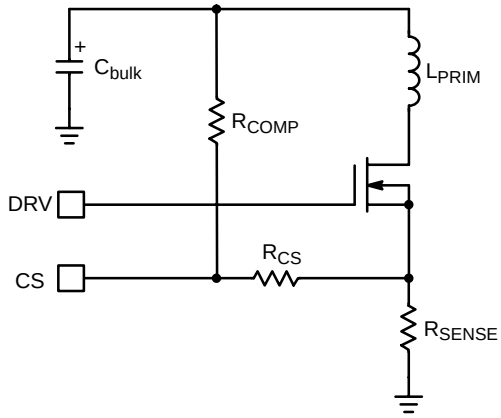


Figure 19. Classical Overpower Compensation

Unfortunately, it is not possible to implement this scheme with NCP1207 as the resistor in series with the current sense information (R_{CS}) has to be low, since it is used to adjust the skip cycle level. It would require a low compensation resistor R_{COMP}, wasting a lot of power.

It would be interesting to have an image of the input voltage, but at a lower level. It is possible by using the forward voltage on the auxiliary winding: by adding a diode in series with the auxiliary winding, we have access to the forward voltage (Figure 20).

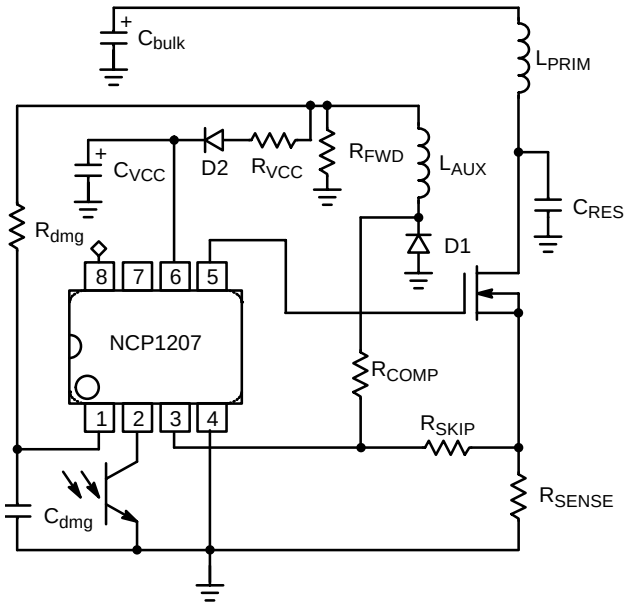


Figure 20. Overpower Compensation using Forward Voltage

This forward voltage is proportional to $N.V_{IN}$ (N being the turn ratio of the windings). R_{FWD} is added to supply the reverse current during the forward activity. Knowing the value of the forward voltage and the series resistor R_{SKIP}, it is then easy to calculate the value of the compensation resistor R_{COMP} to create the desired offset on the current sense signal at high input voltage.

Here are some screen shots describing the effect of the compensation:

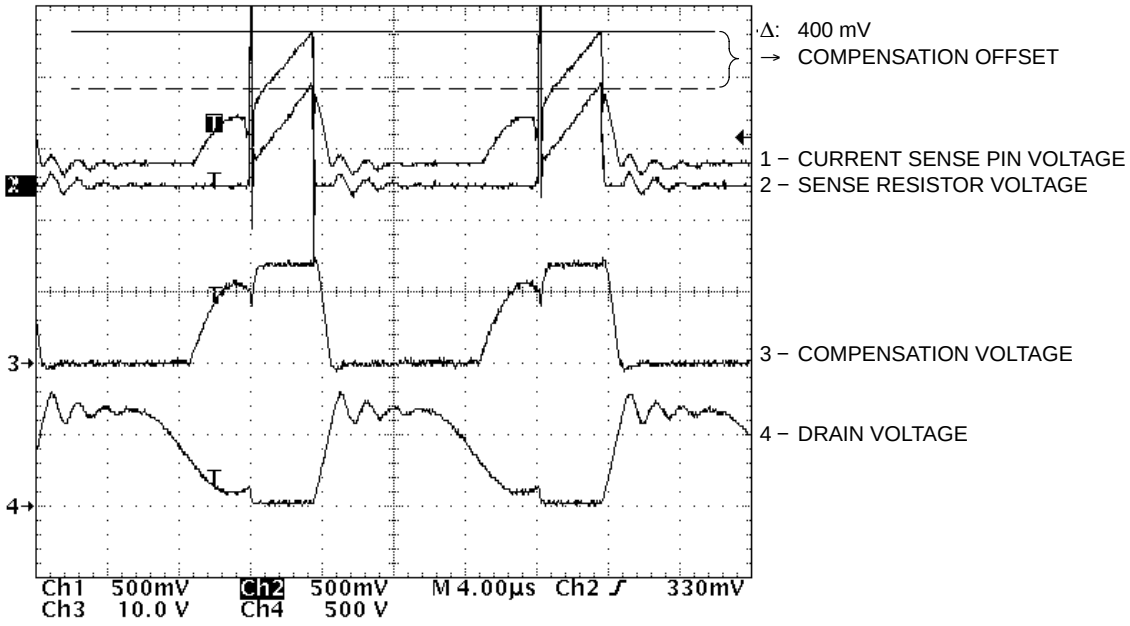


Figure 21. Line Compensation at V_{IN} = 365 Vdc

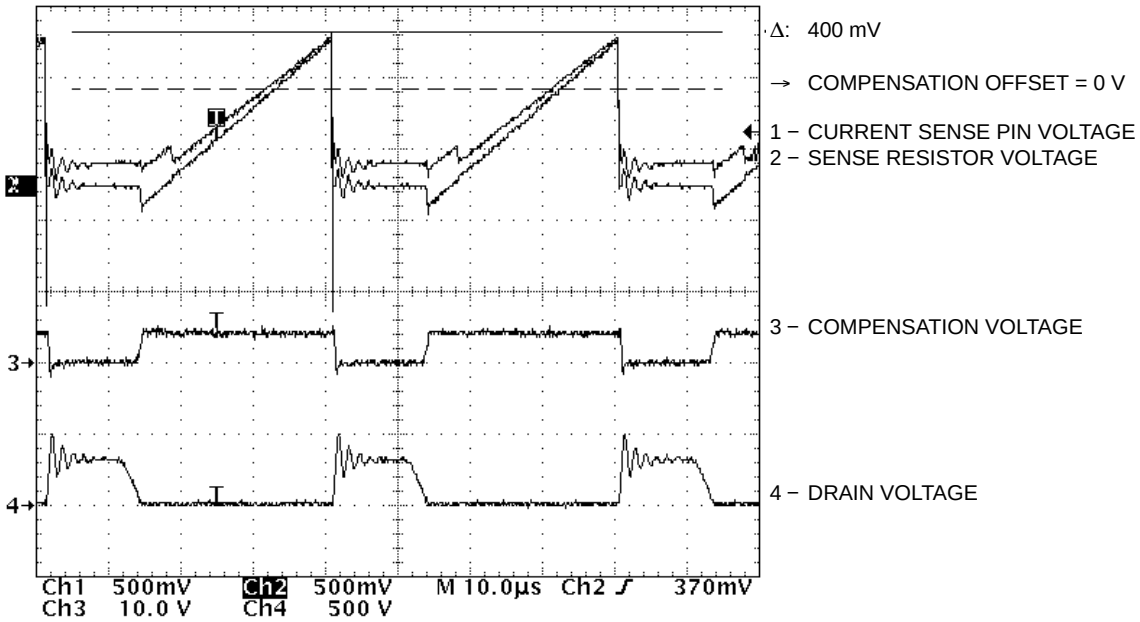


Figure 22. Line Compensation at V_{IN} = 100 Vdc

Approach 2 (Regulation Foldback):

By sensing the current flowing in an output, it is possible to build an efficient overcurrent protection, folding back the regulation level when the current threshold is reached. It is purposely completely independent of the input voltage.

A simple bipolar NPN transistor can sense the voltage across the resistor and pull down the optocoupler emitting diode (Figure 23). The protection is temperature dependent, but it gives enough precision in most applications. The main drawback of this approach is that only one output is protected: the circuitry must be duplicated on each output that needs to be protected.

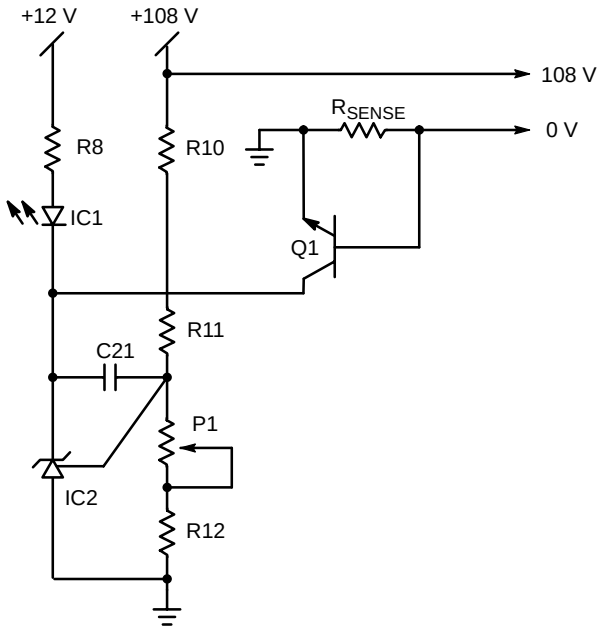


Figure 23. Overcurrent Foldback on the 108 V Output

Final Schematic

Figure 24 on the following page, shows the final schematic implemented on the demonstration board. It includes all the options presented in the design steps.

The board is equipped by default with the following options:

- An RCD clamp for non−ZVS designs
- A regulation by Zener diode when the secondary reconfiguration is activated
- An overcurrent protection on the 108 V output

The PCB also accepts the following options:

- A regulation by the ripple generator when the secondary reconfiguration is activated (see bill of material for components mounting for this option)
- An overpower compensation through the use of the forward voltage on the auxiliary winding

Two types of transformers can be soldered on the board, either from OREGA or from VOGT ELECTRONIC.

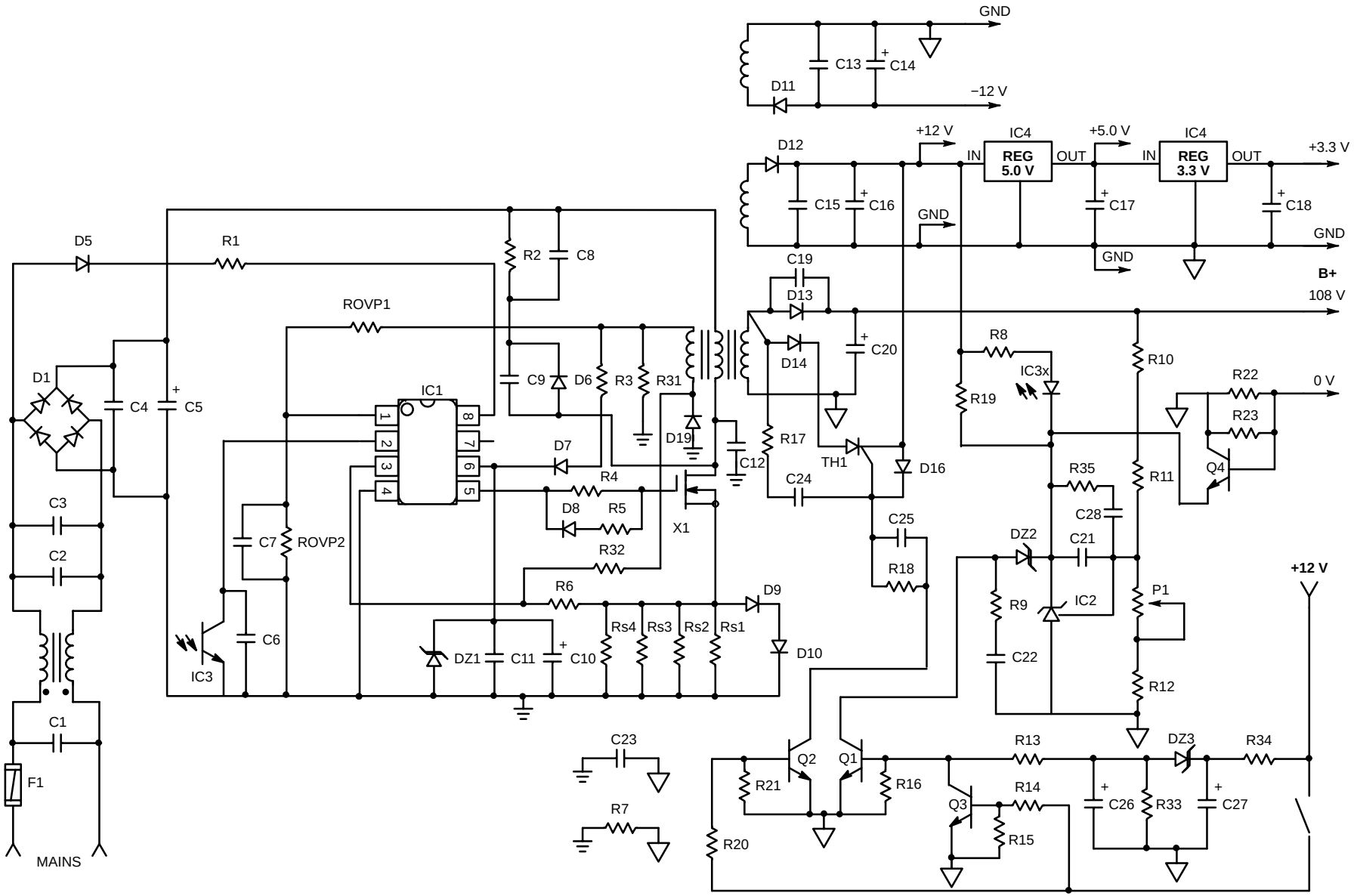


Figure 24. Schematic of the Demonstration Board

Board Performance

Efficiency

At V_{IN} = 250 VAC, POUT = 70 W, η = 84.3%
At V_{IN} = 90 VAC, POUT = 70 W, η = 85.1%
At V_{IN} = 250 VAC, POUT = 65 W, η = 83.6%
At V_{IN} = 90 VAC, POUT = 65 W, η = 84.7%

Standby Power

Measured on an Infratek wattmeter operating in watt−hour accumulation mode for better accuracy (run length = 1 hour). At V_{IN} = 230 VAC, 5.0 V output loaded with 30 mA (i.e. 150 mW output power):

- With simple Zener regulation: **P_{STBY} = 850 mW** (but might be noisy with some transformers)
- With ripple generator: **P_{STBY} = 1.0 W**

Conducted EMI Signature

An EMI test has been conducted on the board, at 110 VAC and 220 VAC, with full load on all the outputs (75 W total secondary power): Figure 25. The measurement is done in quasi−peak (QP) mode.

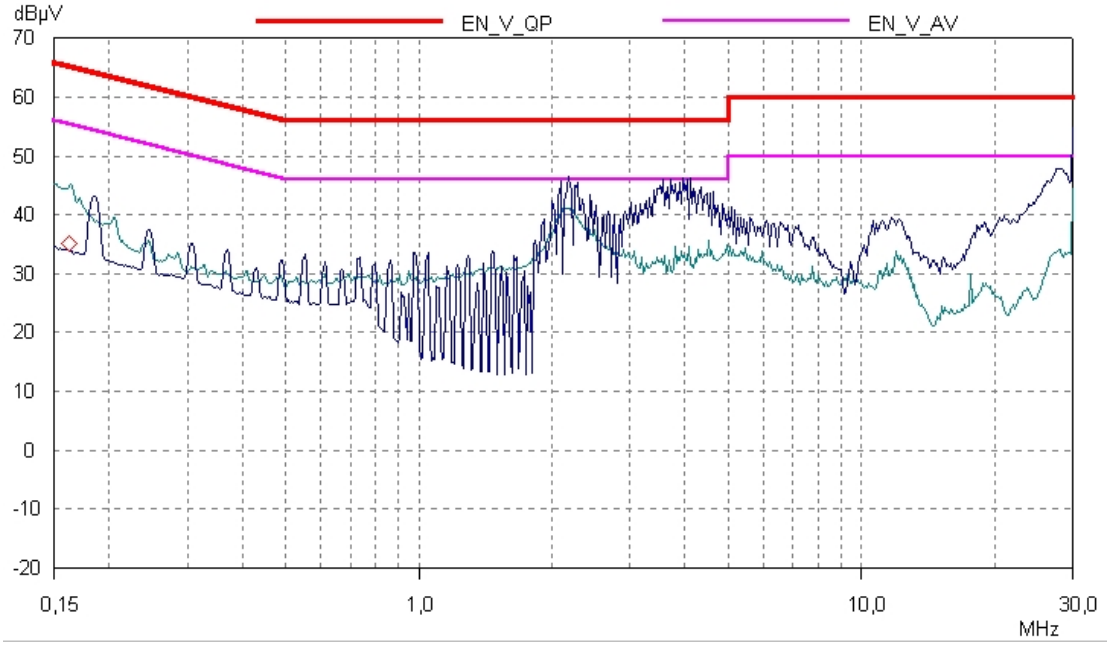


Figure 25. EMI Signature Captured at 110 VAC and 230 VAC

WAVEFORMS

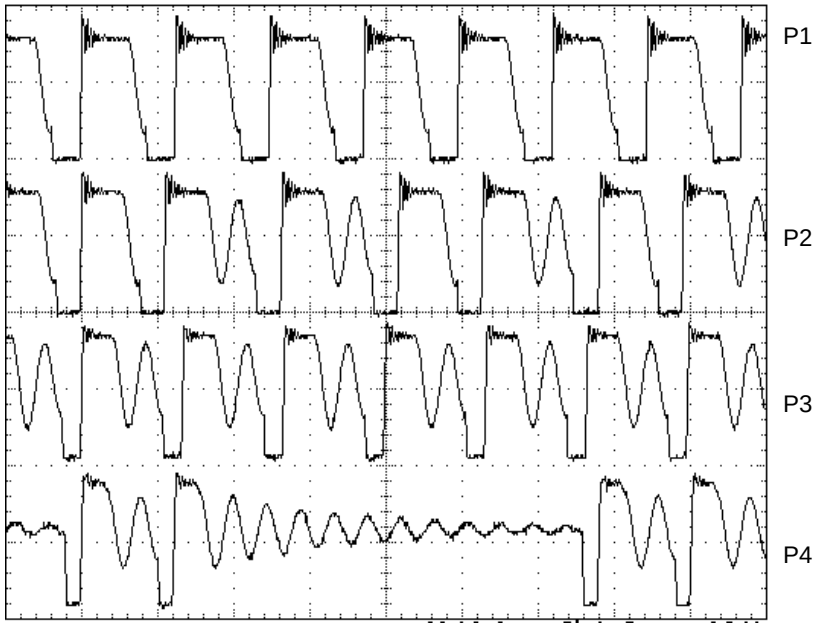


Figure 26. V_{DRAIN} for Different Output Power (P1 > P2 > P3 > P4)

Figure 26 shows valley jumping when output power decreases (P3 < P2 < P1), and skip in case of really light load (P4).

Maximum drain voltage is obtained at high line, full load. At 380 Vdc, 80 W on the output, we can see from Figure 27 that the MOSFET is safe.

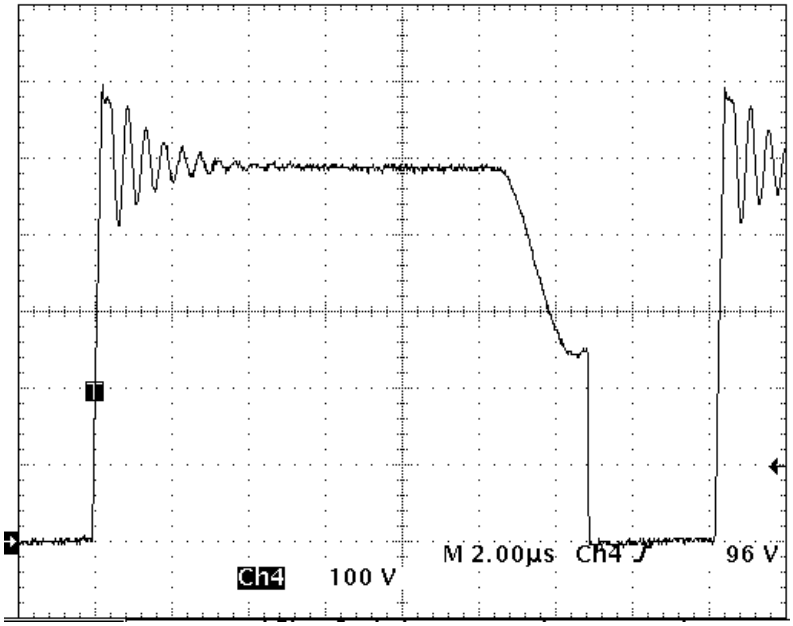


Figure 27. Max V_{DRAIN} at High Line, Full Load

As Figure 28 shows, the transition from standby to normal mode is smooth, without any steps. As the “+12 V” output is still regulated in standby, it can be lowered as much as needed to supply the 5.0 V regulator.

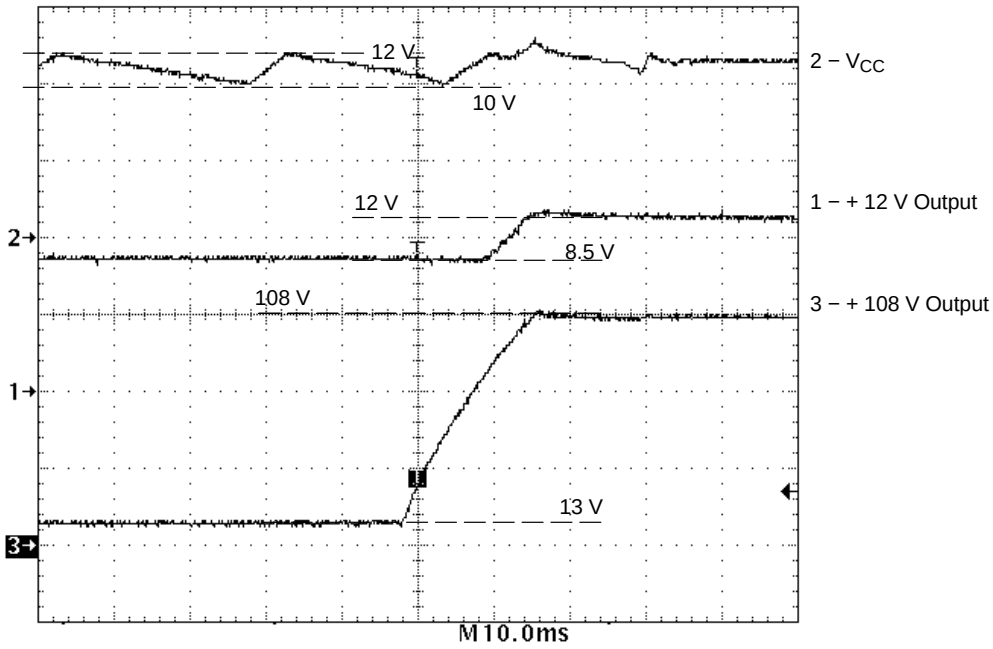


Figure 28. Standby to Normal Mode Transition

BILL OF MATERIAL

Standard Equipment of the Board

GENERIC TABLE

Part Number	Reference
IC1	NCP1207
IC2	TL431
IC3	SFH615
IC4	MC7805
IC5	LP2950−3.3 V
X1	IRFIB6N60
Q1, Q2, Q3, Q4	BC547C
D1	KBU4K
D5, D9, D10	1N4007
D7, D8, D16	1N4148
D6, D14	1N4937
D13	MR856
D11, D12	MR852
D19	Replaced by a wire
DZ1	Zener 15 V
DZ2	Zener 5.6 V
DZ3	Replaced by a wire
TH1	MCR22−6
F1	250 VAC/2.0 A
T1*	Transformer VOGT reference UL030 121/21 or OREGA reference G7209−01
L1	Mains filter OREGA
SW1	TL36P
C1, C2	220 nF/275 VAC classe X2
C3, C4	1 nF/1 kV
C5	150 μF/400 V
C6, 21	1 nF/50 V
C7	82 pF/50 V
C8	10 nF/630 V
C9, C19	220 pF/1 kV
C10	33 μF/50 V
C11, C13, C15, C25, C28	100 nF/50V
C12	330 pF/1 kV
C14, C16	470 μF/35 V
C17, C18	100 μF/16 V
C20	47 μF/250 V
C23	2.2 nF/4 kV classe Y
C24	100 pF/200 V
P1	500 R
Rs1, Rs2, Rs3, Rs4	1.1 R
RVOP1	33 k
R1	15 k
R2	47 k/2 W
R3	47 R
R4	10 R
R5	Replaced by a wire
R6	390 R
R7	4.7 Meg/4 kV
R8, R18, R19	1 k
R10	56 k
R11	47 k
R12	2.2 k
R13, R14, R15, R16, R20, R21	10 k
R17	4.7 k
R22, R23	1.5 R
R34	Replaced by a wire
R35	27 k

*For a ZVS transformer, order OREGA ref. G7209−03 (C22, C26, C27, R9, R31, R32 and R33 are not implemented, a 15 V Zener diode is added in parallel to IC2)

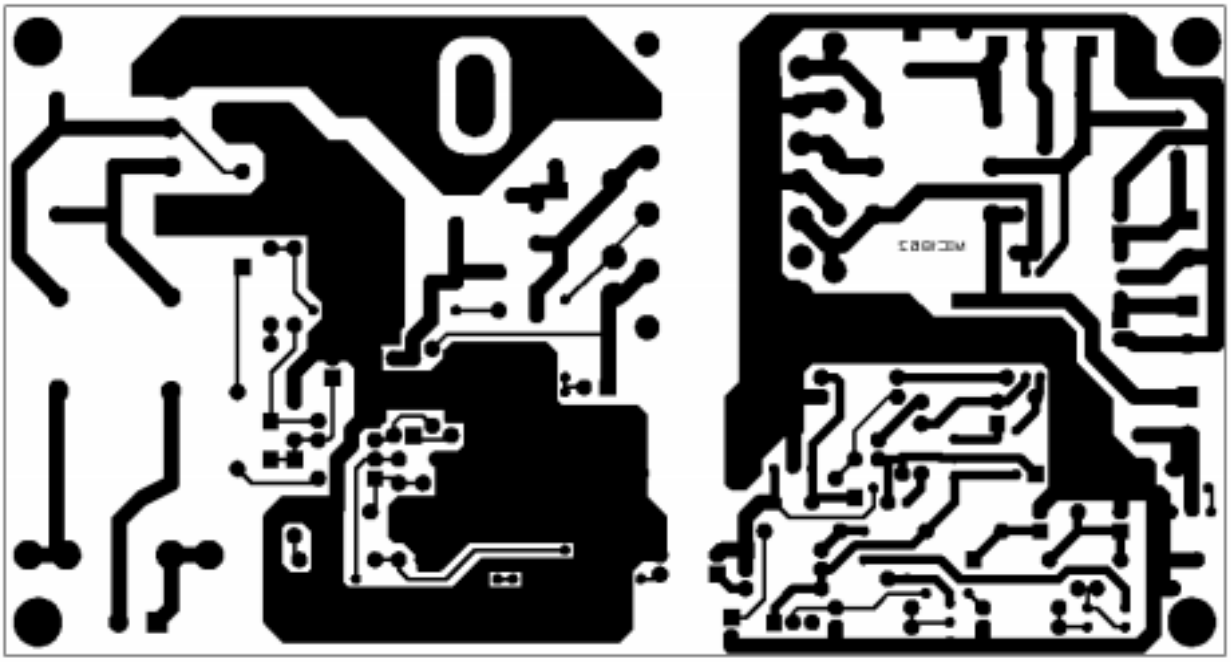
Modifications needed to implement the standby ripple generator:

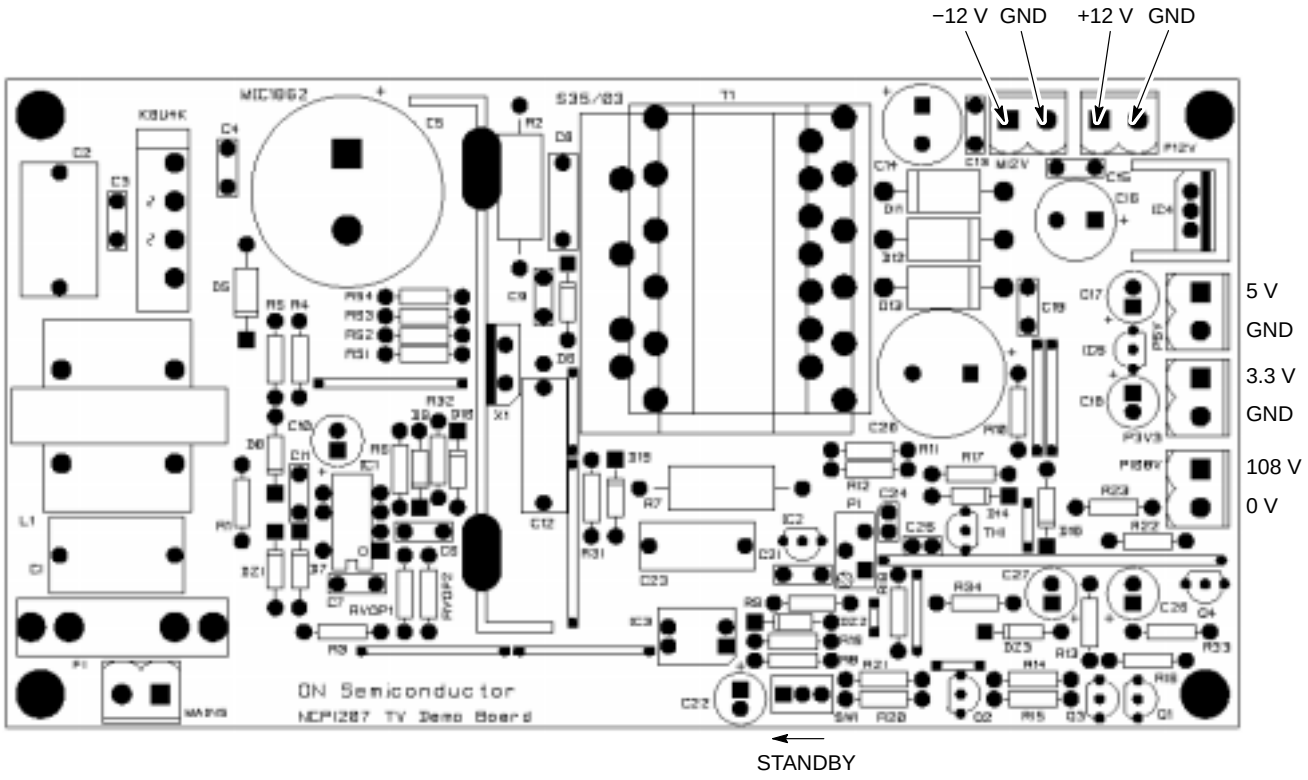
Part Number	Reference
DZ2	Replaced by a wire
DZ3	Zener 3.9 V
C26, C27	1.0 μF/25 V
R13	22 R
R33	15 k
R34	47 k

Overpower Compensation:

Part Number	Reference
D19	1N4148
R31	4.7 k
R32	18 k

PCB LAYOUT





Some important points that have been taken into account to make a proper layout:

- The high alternating current loops areas both on primary and secondary are the smallest possible to minimize noise and EMI emission
- The drain track is the shortest possible
- The heatsink is connected to ground. It acts as a shield between the noisy signals (drain, RCD clamp, transformer) and the sensitive signals around the controller

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